PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-224033
(43)Date of publication of application : 26.08.1997

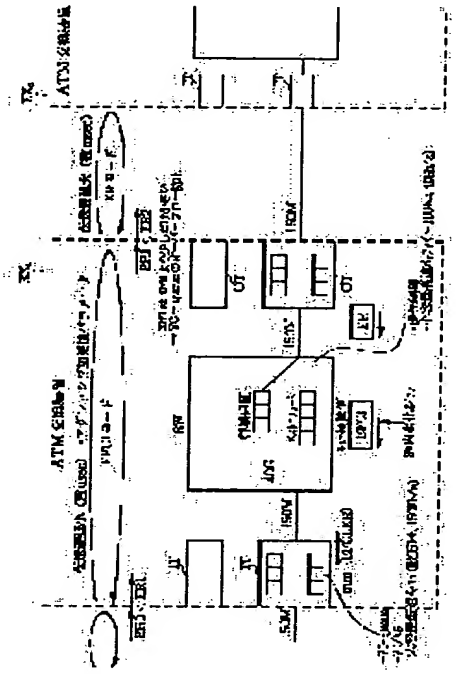
(51)Int.CI. H04L 12/28
H04Q 3/00

(21)Application number : 08-029545
(22)Date of filing : 16.02.1996

(71)Applicant : NIPPON TELEGR & TELEPH CORP <NTT>
(72)Inventor : SHIOMOTO KOHEI
YAMANAKA NAOAKI
HASEGAWA HARUHISA

(54) ATM EXCHANGE DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To accelerate a core switch and to perform high-accuracy congestion control by controlling the speed of cell to be sent out to the core switch according to transmission speed designation information.
SOLUTION: An output line dealing part OT is provided with an ER arithmetic part for operating an ER based on an EFCI added to a cell coming from a core switch SW and for loading that ER to an RM cell to be returned and an input line dealing part IT is provided with a read control part 5 for controlling the speed of cell to be sent out to the core switch SW according to the ER loaded on the RM cell returned from the output line dealing part OT. A high-speed buffer BUH is provided with a band guarantee class buffer and a best effort class buffer corresponding to the priority of cells and adds the EFCI to an EFCI adding part 30 corresponding to the queue length of the best effort class buffer. As long as the cell exists in the band guarantee buffer, this buffer is serviced and only when this buffer is empty, the best effort class buffer is serviced.



LEGAL STATUS

[Date of request for examination]	04.01.1999
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3059100
[Date of registration]	21.04.2000
[Number of appeal against examiner's decision	

of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平9－224033

(43)公開日　平成９年(1997)８月26日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０４Ｌ　12/28		9466－5Ｋ	Ｈ０４Ｌ　11/20	Ｇ	
Ｈ０４Ｑ　3/00			Ｈ０４Ｑ　3/00		

審査請求　未請求　請求項の数４　ＯＬ　（全９頁）

(21)出願番号　特願平8－29545

(22)出願日　平成８年(1996)２月16日

(71)出願人　000004226
日本電信電話株式会社
東京都新宿区西新宿三丁目19番２号

(72)発明者　塩本　公平
東京都新宿区西新宿三丁目19番２号　日本電信電話株式会社内

(72)発明者　山中　直明
東京都新宿区西新宿三丁目19番２号　日本電信電話株式会社内

(72)発明者　長谷川　治久
東京都新宿区西新宿三丁目19番２号　日本電信電話株式会社内

(74)代理人　弁理士　井出　直孝　（外１名）

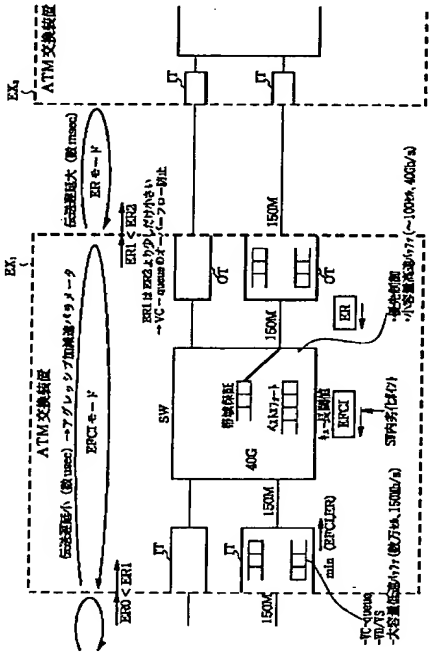
(54)【発明の名称】　ＡＴＭ交換装置

(57)【要約】

【課題】　ＡＴＭ交換装置で、高速で動作することが要求されるコアスイッチの構成を簡単化しつつ高い精度の輻輳制御を行う。

【解決手段】　伝送遅延が小さいＡＴＭ交換装置内では、コアスイッチの構成を複雑化しないＥＦＣＩモードによる輻輳制御を行い、伝送遅延が大きいＡＴＭ交換装置相互間では、精度の高いＥＲモードによる輻輳制御を行う。

【効果】　コアスイッチを高速化することができるとともに、ＡＴＭ通信網全体では高い精度の輻輳制御を実現できる。



1

【特許請求の範囲】

【請求項１】　出力回線別の高速バッファと、入力セルの宛先別にこのバッファに入力セルを分配する手段とを有するコアスイッチ（ＳＷ）を備え、このコアスイッチの入力側に低速バッファを有する入力回線対応部（ＩＴ）が複数設けられ、このコアスイッチの出力側に低速バッファを有する出力回線対応部（ＯＴ）が複数設けられたＡＴＭ交換装置において、

前記入力回線対応部（ＩＴ）には、入力回線から到来するＲＭセルに送出速度指定情報（ＥＲ情報）を搭載してそのＲＭセルの発生元に向け折り返す手段と、一定数のセル通過毎に新しいＲＭセルを前記コアスイッチに向けて送出する手段とを備え、

前記出力回線対応部（ＯＴ）には、コアスイッチから到来するＲＭセルに輻輳情報を搭載してそのＲＭセルの発生元に向け前記コアスイッチに折り返す手段と、一定セル通過毎に新しいＲＭセルを出力回線に送出する手段と、後段の入力回線対応部により折り返されたこのＲＭセルに搭載された送出速度指定情報（ＥＲ情報）にしたがって前記出力回線に送出するセルの速度を制御する手段とを備え、

前記コアスイッチ（ＳＷ）には、通過するセルに前記高速バッファのキュー長に応じて輻輳の有無を示す情報（ＥＦＣＩ情報）を付加する手段を備え、

前記出力回線対応部（ＯＴ）には、前記コアスイッチから到来するセルに付加された輻輳の有無を示す情報（ＥＦＣＩ情報）を演算して折り返すＲＭセルにその送出速度指定情報（ＥＲ情報）を搭載する手段を備え、

前記入力回線対応部（ＩＴ）では前記出力回線対応部から折り返されたＲＭセルに搭載された送出速度指定情報（ＥＲ情報）にしたがって前記コアスイッチに送出するセルの速度を制御する手段を備えたことを特徴とするＡＴＭ交換装置。

【請求項２】　前記高速バッファは、セルの優先順位に対応して複数設けられ、前記情報を付加する手段は、優先順位が第二位以降の高速バッファのキュー長に応じて輻輳の有無を示す情報を付加する請求項１記載のＡＴＭ交換装置。

【請求項３】　前記出力回線対応部（ＯＴ）およびまたは前記入力回線対応部（ＩＴ）で折り返すＲＭセルに搭載する送出速度指定情報（ＥＲ情報）は、その回線対応部の低速バッファのキュー長から判断される受入れ可能な速度に一定比率を乗じた遅い速度である請求項１記載のＡＴＭ交換装置。

【請求項４】　前記入力回線対応部（ＩＴ）および前記出力回線対応部（ＯＴ）の各低速バッファのキュー長の判定を行う手段および前記ＲＭセルの識別手段はバーチャルチャネル対応に設けられる請求項１ないし３のいずれかに記載のＡＴＭ交換装置。

【発明の詳細な説明】

2

【０００１】

【発明の属する技術分野】本発明はＡＴＭ(Asynchronous Transfer Mode:非同期転送モード）に利用する。本発明はＡＴＭ通信網の輻輳制御技術に関する。

【０００２】

【従来の技術】従来のＡＴＭ交換装置を図８を参照して説明する。図８は従来のＡＴＭ交換装置の概念図である。ＡＴＭ交換装置は複数の入力回線対応部ＩＴと出力回線対応部ＯＴとコアスイッチＳＷからなる。コアスイッチＳＷは１セル時間毎に全ての入力回線対応部ＩＴから送出されるセルをセルヘッダの内容にしたがって所望の出力回線対応部ＯＴに転送するものである。ここで、同時に複数の入力回線対応部ＩＴから同一出力回線対応部ＯＴを目指すセルが入力された場合はコアスイッチＳＷの出力バッファＢＵで待ち合わせが発生する。このように従来のＡＴＭ交換装置ではコアスイッチＳＷの出力バッファＢＵが輻輳が発生するポイントになる。

【０００３】図９は従来のＡＴＭ網におけるＡＢＲ(Available Bit Rate)によるレート制御を説明する図である。ＡＢＲでは、ＲＭ(Resouce Management)セルを発側端末から送出し、着側でＲＭセルを折り返して発側に戻ってくる過程において、網の輻輳状態に応じた制御情報をＲＭセルに搭載することにより発側端末がセルの送出レートを制御するものである。このようにＡＢＲでは発側端末と着側端末の間でセルの送出レートを計算するための制御ループがＲＭセルの送受により形成されている。セル送出レートの制御方法に関してはＥＦＣＩ(Explicit Forward Congestion Indication)モードとＥＲ(Explicit Rate) モードがある。

【０００４】図９（ａ）に示すように、ＥＦＣＩモードでは網内のＡＴＭ交換装置のコアスイッチの出力バッファで輻輳を検出したら、輻輳したことを示すためセルのＥＦＣＩフィールドをセットして着側端末に通知し、着側端末が発側に折り返すＲＭセルに輻輳情報を示すためＣＩフィールドをセットして発側端末に通知する。発側端末のセルの送出レートは着側端末から折り返されるＲＭセルのＣＩフィールドがセットされていない限り所定の上昇率にしたがって上昇させ、ＣＩフィールドがセットされていると所定の減少率にしたがって減少させる。

【０００５】図９（ｂ）に示すように、ＥＲモードでは網内のＡＴＭ交換装置のコアスイッチの出力バッファで輻輳を検出したら、ＲＭセルにＥＲ情報すなわち送出速度指定情報を明示して、発側端末にセルの送出レートを示すものである。このときの送出速度指定情報は公平性を保つことと輻輳が収まることの２条件から各ＶＣ毎に値が計算される。つまり、ＥＲモードでは網内の輻輳したＡＴＭ交換装置のコアスイッチが各ＶＣ毎のセルの送出レートを計算するのに対し、ＥＦＣＩモードでは網内の輻輳したＡＴＭ交換装置のコアスイッチは輻輳したことを示すのみでセルの送出レートの計算は端末側に委ね

られる。

【０００６】

【発明が解決しようとする課題】公衆網のように往復の伝搬遅延時間が大きい網ではＥＦＣＩモードで動作すると、スループットが向上しないことや公平性の問題が顕著になるので、ＥＲモードで動作させた方が望ましいことがわかっている。しかしながら、ＥＲモードは網内の輻輳したＡＴＭ交換装置のコアスイッチの出力バッファで各ＶＣ毎にセルの送出レートを計算する必要があるが、一般に網内のＡＴＭ交換装置のコアスイッチは高速で動作するので、ＶＣ毎のセル送出レートを計算するのは困難である。特に、ＡＴＭ交換装置の規模が大きくなると、その困難さは顕著になる。また、伝搬遅延が大きくなるにしたがって、高いスループットを得るために大容量のバッファが必要となるが、高速で動作するコアスイッチに大容量のバッファを配備するのは一般的に困難である。

【０００７】また、ＡＴＭ網においてはＡＢＲだけでなく、ＣＢＲ(Constant Bit Rate)、ＶＢＲ(Variable Bit Rate)などのサービスクラスが存在し、それらはＡＢＲトラヒックにより影響を受けないように帯域を保証する必要がある。

【０００８】本発明は、このような背景に行われたものであって、コアスイッチの構成および動作を複雑にすることなく高いスループットと公平性を維持することができるＡＴＭ交換装置を提供することを目的とする。本発明は、セルの優先順位に応じて設けられたサービスクラスが相互に干渉することのない輻輳制御が行えるＡＴＭ交換装置を提供することを目的とする。

【０００９】

【課題を解決するための手段】コアスイッチの各出力回線において、帯域保証クラス用のバッファが完全優先で転送される。つまり、帯域保証クラスのバッファにセルがある限り、帯域保証クラスのバッファがサービスされ、帯域保証クラスのバッファが空のときだけベストエフォートクラスのバッファがサービスされる。

【００１０】ベストエフォートクラスの負荷が高くなると、ベストエフォートクラスのバッファのキュー長が伸びていくので、キュー長がある一定の閾値を超えると、通過セルのＥＦＣＩ(Explicit Forward Congestion Indication)フィールドをセットする。

【００１１】出力回線対応部ではコアスイッチからのセルにＥＦＣＩがセットされているとコアスイッチの出力バッファが輻輳していることを知るので、入力回線対応部からＲＭセルが送出されてくると、輻輳表示フィールドに輻輳状態である旨をセットして折り返す。また、その際、出力回線対応部のバッファのキュー長が閾値を超えている場合にも輻輳表示フィールドに輻輳状態である旨をセットして折り返す。また、出力回線対応部は一定セル数通過毎にＲＭセルを生成し、そのＥＲフィールドにバッファからのセル送出レートをセットして、後段の網に送出する。後段の網から折り返されてきたＲＭセルの輻輳表示フィールドの値にしたがってバッファからのセル送出レートを調整する。

【００１２】入力回線対応部では輻輳状態である旨を通知するＲＭセルが出力回線対応部から返送されてくると所定の減少率でバッファからのセル送出レートを減少させる。また、ＲＭセルが輻輳状態を示していなければ所定の上昇率でセル送出レートを上昇させる。また、入力回線対応部はバッファのキュー長が閾値を超えた場合には前段の網から送出されてくるＲＭセルの輻輳表示フィールドに輻輳状態である旨をセットして折り返す。

【００１３】出力回線対応部および入力回線対応部から送信されたＲＭセルを折り返す際に、輻輳表示フィールドに値をセットするのに加え、出力回線対応部のバッファからのセル送出レートに所定の率を乗じたものをＲＭセルのＥＲフィールドにセットして折り返す。また、後段の網から折り返されたＲＭセルの輻輳表示フィールドの値にしたがって計算したバッファからのセル送出レートとＲＭセルのＥＲフィールドに設定された速度の小さい方でバッファからセルを送出する。

【００１４】入力回線対応部ではセル送出レートを計算する際に、セル送出レートは出力回線対応部から返送されてきたＲＭセルのＥＲフィールドの値以下の値で設定される。また、入力回線対応部は前段の網から送出されてくるＲＭセルを折り返す際に、輻輳表示フィールドをセットするのに加え、ＥＲフィールドにバッファからの読出速度に所定の率を乗じた値をセットして、前段の網にＲＭセルを折り返す。

【００１５】このように制御することによって、セル送出レートは、上流ノードに遅るにしたがって低く抑えられ、輻輳状態に陥ることを回避することができる。

【００１６】すなわち、本発明はＡＴＭ交換装置であって、出力回線別の高速バッファと、入力セルの宛先別にこのバッファに入力セルを分配する手段とを有するコアスイッチ（ＳＷ）を備え、このコアスイッチの入力側に低速バッファを有する入力回線対応部（ＩＴ）が複数設けられ、このコアスイッチの出力側に低速バッファを有する出力回線対応部（ＯＴ）が複数設けられたＡＴＭ交換装置である。

【００１７】ここで、本発明の特徴とするところは、前記入力回線対応部（ＩＴ）には、入力回線から到来するＲＭセルに送出速度指定情報（ＥＲ情報）を搭載してそのＲＭセルの発生元に向け折り返す手段と、一定数のセル通過毎に新しいＲＭセルを前記コアスイッチに向けて送出する手段とを備え、前記出力回線対応部（ＯＴ）には、コアスイッチから到来するＲＭセルに輻輳情報を搭載してそのＲＭセルの発生元に向け前記コアスイッチに折り返す手段と、一定セル通過毎に新しいＲＭセルを出力回線に送出する手段と、後段の入力回線対応部により

折り返されたこのＲＭセルに搭載された送出速度指定情報（ＥＲ情報）にしたがって前記出力回線に送出するセルの速度を制御する手段とを備え、前記コアスイッチ（ＳＷ）には、通過するセルに前記高速バッファのキュー長に応じて輻輳の有無を示す情報（ＥＦＣＩ情報）を付加する手段を備え、前記出力回線対応部（ＯＴ）には、前記コアスイッチから到来するセルに付加された輻輳の有無を示す情報（ＥＦＣＩ情報）を演算して折り返すＲＭセルにその送出速度指定情報（ＥＲ情報）を搭載する手段を備え、前記入力回線対応部（ＩＴ）では前記出力回線対応部から折り返されたＲＭセルに搭載された送出速度指定情報（ＥＲ情報）にしたがって前記コアスイッチに送出するセルの速度を制御する手段を備えたところにある。

【００１８】これにより、コアスイッチの構成および動作を複雑にすることなく高いスループットと公平性を維持することができる。

【００１９】前記高速バッファは、セルの優先順位に対応して複数設けられ、前記情報を付加する手段は、優先順位が第二位以降の高速バッファのキュー長に応じて輻輳の有無を示す情報を付加することが望ましい。

【００２０】これにより、セルの優先順位に応じて設けられたサービスクラスが相互に干渉することのない輻輳制御が行える。

【００２１】前記出力回線対応部（ＯＴ）およびまたは前記入力回線対応部（ＩＴ）で折り返すＲＭセルに搭載する送出速度指定情報（ＥＲ情報）は、その回線対応部の低速バッファのキュー長から判断される受入れ可能な速度に一定比率を乗じた遅い速度であることが望ましい。

【００２２】これにより、セル送出レートは、上流ノードに遅るにしたがって低く抑えられ、輻輳状態に陥ることを回避することができる。

【００２３】前記入力回線対応部（ＩＴ）および前記出力回線対応部（ＯＴ）の各低速バッファのキュー長の判定を行う手段および前記ＲＭセルの識別手段はバーチャルチャネル対応に設けられることが望ましい。

【００２４】これにより、バーチャルチャネル対応にきめ細かい輻輳制御を行うことができる。

【００２５】

【発明の実施の形態】

【００２６】

【実施例】本発明実施例の構成を図１ないし図４を参照して説明する。図１は本発明実施例の全体構成図である。図２はコアスイッチのブロック構成図である。図３は入力回線対応部のブロック構成図である。図４は出力回線対応部のブロック構成図である。

【００２７】本発明は図１に示すようなＡＴＭ交換装置EX_1、EX_2であって、図２に示すように、出力回線別の高速バッファBU_Hと、入力セルの宛先別にこの高速バッファBU_Hに入力セルを分配する手段としてのセル分配器Ｄとを有するコアスイッチＳＷを備え、このコアスイッチＳＷの入力側に、図３に示すように、低速バッファBU_Lを有する入力回線対応部ＩＴが複数設けられ、このコアスイッチＳＷの出力側に低速バッファBU_Lを有する出力回線対応部ＯＴが複数設けられたＡＴＭ交換装置EX_1、EX_2である。

【００２８】ここで、本発明の特徴とするところは、入力回線対応部ＩＴには、入力回線から到来するＲＭセルに送出速度指定情報であるＥＲを搭載してそのＲＭセルの発生元に向け折り返す手段としてのＲＭセル処理部１およびＥＲ演算部４と、一定数のセル通過毎に新しいＲＭセルをコアスイッチＳＷに向けて送出する手段としてのＲＭセル生成部３およびＲＭセル処理部２とを備え、出力回線対応部ＯＴには、コアスイッチＳＷから到来するＲＭセルに輻輳情報を搭載してそのＲＭセルの発生元に向けコアスイッチＳＷに折り返す手段としてのＲＭセル処理部２１と、一定セル通過毎に新しいＲＭセルを出力回線に送出する手段としてのＲＭセル生成部２３およびＲＭセル処理部２２と、後段の入力回線対応部ＩＴにより折り返されたこのＲＭセルに搭載されたＥＲにしたがって前記出力回線に送出するセルの速度を制御する手段としての読出制御部２５とを備え、コアスイッチＳＷには、通過するセルに高速バッファBU_Hのキュー長に応じて輻輳の有無を示す情報であるＥＦＣＩを付加する手段としてのＥＦＣＩ付加部３０を備え、出力回線対応部ＯＴには、コアスイッチＳＷから到来するセルに付加されたＥＦＣＩに基づいて演算し折り返すＲＭセルにそのＥＲを搭載する手段としてのＥＲ演算部２４を備え、入力回線対応部ＩＴでは出力回線対応部ＯＴから折り返されたＲＭセルに搭載されたＥＲにしたがってコアスイッチＳＷに送出するセルの速度を制御する手段としての読出制御部５を備えたところにある。

【００２９】高速バッファBU_Hは、セルの優先順位に対応して帯域保証クラスバッファおよびベストエフォートクラスバッファの二つのバッファが設けられ、ＥＦＣＩ付加部３０は、ベストエフォートクラスバッファのキュー長に応じてＥＦＣＩを付加する。

【００３０】次に、本発明実施例の動作を説明する。図２に示すコアスイッチＳＷの各出力回線では帯域保証クラスバッファが完全優先で転送される。つまり、帯域保証クラスバッファにセルがある限り、帯域保証クラスバッファがサービスされ、帯域保証クラスバッファが空のときだけベストエフォートクラスバッファがサービスされる。

【００３１】ベストエフォートクラスバッファの負荷が高くなると、ベストエフォートクラスバッファのキュー長が伸びていくので、キュー長がある一定の閾値を超えると、通過セルのＥＦＣＩフィールドをセットする。

【００３２】図４に示す出力回線対応部ＯＴはコアスイ

ッチＳＷからセルを受信する。セルはＲＭセルと非ＲＭセルがある。ＲＭセルはコアスイッチＳＷに向けて折り返されて、非ＲＭセルが出力回線対応部ＯＴの低速バッファBU_Lでバッファリングされ後段の網に向けてＶＣ毎の所定のレートで低速バッファBU_Lから送出されていく、折り返されるＲＭセルに搭載される情報はＣＩとＥＲがあるが、それぞれ、それらはコアスイッチＳＷの輻輳状態と出力回線対応部ＯＴの低速バッファBU_Lのセル送出レートにより決定される。

【００３３】図５は出力回線対応部ＯＴのセル受信時の動作を示すフローチャートである。出力回線対応部ＯＴに到着したセルがあり（Ｓ１）、その到着したセルのＶＣＩがｉのとき（Ｓ２）、そのセルが非ＲＭセルであり（Ｓ３）、ＥＦＣＩがセットされていれば（Ｓ４）、コアスイッチＳＷが輻輳中であると判定する（Ｓ５）。そのセルは出力回線対応部ＯＴの低速バッファBU_Lにバッファリングされ、ＶＣ毎の所定のレートで読出される（Ｓ６）。

【００３４】また、到着したセルがＶＣＩ＝ｉのＲＭセルであり（Ｓ３）、出力回線対応部ＯＴの低速バッファ＊

$$ACR_i = ACR_i \ (1 - RDF_i) \quad \cdots (1)$$

として減少させ、ＣＩフィールドがセットされていなけ※　※れば、

$$ACR_i = ACR_i + NAIR_i \quad \cdots (2)$$

として低速バッファBU_Lからのセルの送出レートを増加させる。

【００３６】ここで、RDF_iは事前に決まっているＶＣＩ＝ｉの減少レートであり、$NAIR_i$は事前に決まっているＶＣＩ＝ｉの増加レートである。いずれの場合もACR_iは折り返されたＲＭセルに搭載されているＥＲ値ER_iよりも小さい値に設定される。

【００３７】図３に示す入力回線対応部ＩＴのＲＭセル処理部２およびＲＭセル生成部３はＶＣ単位に一定セル数通過毎にＲＭセルを生成して出力回線対応部ＯＴに向★

$$ACR_i = ACR_i \ (1 - RDF_i) \quad \cdots (3)$$

として減少させる（Ｓ１６）。ここで、RDF_iは事前に決まっているＶＣＩ＝ｉの減少レートである。ＣＩフィールドがセットされていなければ（Ｓ１３）、コアス☆

$$ACR_i = ACR_i + NAIR_i \quad \cdots (4)$$

として増加させる（Ｓ１４）。ここで、$NAIR_i$は事前に決まっているＶＣＩ＝ｉの増加レートである。いずれの場合もACR_iは折り返されたＲＭセルに搭載されているＥＲ値ER_iよりも小さい値に設定される（Ｓ１５）。

【００３９】また、図３において入力回線対応部ＩＴのＲＭセル処理部１は前段の網から送出されてくるＲＭセルを前段の網に向けて折り返す。このとき、ＥＲフィールドに当該ＶＣの低速バッファBU_Lからのセル送出レートに所定の率を乗じた値をセットして前段の網にＲＭセルを折り返す。

【００４０】以上のようにコアスイッチＳＷ、入力回線＊BU_Lのキュー長が閾値を超えたかコアスイッチＳＷが輻輳中であれば（Ｓ７）、さらにCI_i＝１をセットし（Ｓ８）、ER_i＝ａACR_iをセットし（Ｓ９）、ＲＭセルをコアスイッチに折り返す（Ｓ１０）。ここで、ACR_iは出力回線対応部ＯＴの低速バッファBU_LからのＶＣＩ＝ｉのセル送出レートであり、ａは安全係数である。

【００３５】また、図４において、出力回線対応部ＯＴのＲＭセル生成部２３およびＲＭセル処理部２２はＶＣ単位に一定セル数通過毎にＲＭセルを後段の網に送出する。その際、そのＥＲフィールドに当該ＶＣのセルの低速バッファBU_Lからのセル送出レートをセットして後段の網に送出する。出力回線対応部ＯＴの読出制御部２５は後段の網から折り返されたＲＭセルのＣＩフィールドとＥＲフィールドにしたがって、低速バッファBU_Lからのセルの送出レートを決定する。すなわち、受信したのがＶＣＩ＝ｉのＲＭセルであるとき、ＣＩフィールドがセットされていれば、低速バッファBU_Lからのセルの送出レートACR_iを

対応部ＩＴ、出力回線対応部ＯＴが動作することにより、図１に示すＡＴＭ交換装置EX_1、EX_2は以下のように機能する。ＡＴＭ交換装置EX_1、EX_2内においてはＡＢＲの制御はＥＦＣＩモードで動作する。ＡＴＭ交換装置EX_1、EX_2の装置内では伝送遅延が小さいので、ＥＦＣＩモードを用いてもスループット低下や公平性に関する問題は発生しない。基本的にはＥＦＣＩモードで動作するが、ただし、ＲＭセルのＥＲフィールドを用いて出力回線対応部ＯＴの低速バッファBU_Lからのセル送出レートより小さい値が入力回線対応部ＩＴに通知される。これにより、入力回線対応部ＩＴの低速バッファBU_Lからのセル送出レートは出力回線対応部

ＯＴの低速バッファBU_Lからセル送出レート以下に制御される。

【００４１】ＡＴＭ交換装置EX_1、EX_2間においてはＡＢＲの制御はＥＲモードで動作する。後段のＡＴＭ交換装置EX_2の入力回線対応部ＩＴの低速バッファBU_Lからのセル送出レートが既に判っているので、ＲＭセルのＥＲフィールドを用いて、容易に前段のＡＴＭ交換装置EX_1に通知することができ、ＡＴＭ交換装置EX_1の出力回線対応部ＯＴの低速バッファBU_Lからのセル送出レートを指定することができる。ＡＴＭ交換装置EX_1の出力回線対応部ＯＴの低速バッファBU_Lからのセル送出レートはＡＴＭ交換装置EX_2の入力回線対応部ＩＴの低速バッファBU_Lからのセル送出レートよりわずかに小さい値に設定される。これにより、ＡＴＭ交換装置EX_2の入力回線対応部ＩＴの低速バッファBU_Lからのセルのオーバーフローを抑制することが可能となる。

【００４２】図７は網内のＡＢＲの制御ループのセルレートの関係を示す図である。後段から前段に遡るにしたがって、ＥＲの値は小さく設定される。また、ＡＴＭ交換装置EX_1内においてはＥＦＣＩモードで計算される値$ACR1_{EFCI}$と後段から通知されるＥＲ２により求まる$ACR1_{ER}$の小さい方に設定される。

【００４３】本発明によれば、ＡＢＲの制御ループはＡＴＭ交換装置ＥＸ内に閉じており、装置内ではＥＦＣＩモードのみで動作させているので、コアスイッチＳＷを簡単にすることができ、かつ伝送遅延が小さいので高いスループットと公平性が得られる効果がある。ＡＴＭ交換装置ＥＸ間ではＥＲモードで動作させているので、伝送遅延が大きいことによるスループットの低下を低く抑えることが可能である。入力回線対応部ＩＴおよび出力回線対応部ＯＴは動作速度がコアスイッチＳＷよりも速くないので、市販のメモリが使用可能であり、大容量の低速バッファBU_Lが容易に実現可能であり、伝送遅延が大きいことによるスループットの低下を抑えることが可能である。

【００４４】また、ＡＴＭ交換装置ＥＸ内のコアスイッチＳＷではＣＢＲやＶＢＲの帯域保証クラスを完全優先で転送するので、ＡＢＲトラヒックの影響を受けることなくサービスを提供することができる。

【００４５】

【発明の効果】以上説明したように、本発明によれば、コアスイッチの構成および動作を複雑にすることなく高いスループットと公平性を維持することができる。また、セルの優先順位に応じて設けられたサービスクラスが相互に干渉することのない輻輳制御が行える。

【図面の簡単な説明】

【図１】本発明実施例の全体構成図。

【図２】コアスイッチのブロック構成図。

【図３】入力回線対応部のブロック構成図。

【図４】出力回線対応部のブロック構成図。

【図５】出力回線対応部のセル受信時の動作を示すフローチャート。

【図６】入力回線対応部の折り返されたＲＭセル受信時の動作のフローチャート。

【図７】網内のＡＢＲの制御ループのセルレートの関係を示す図。

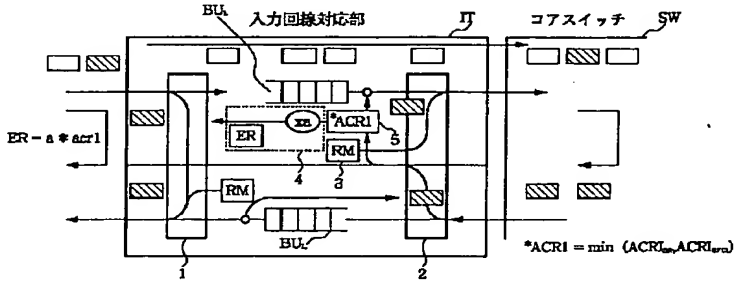
【図８】従来のＡＴＭ交換装置の概念図。

【図９】従来のＡＴＭ網におけるＡＢＲによるレート制御を説明する図。

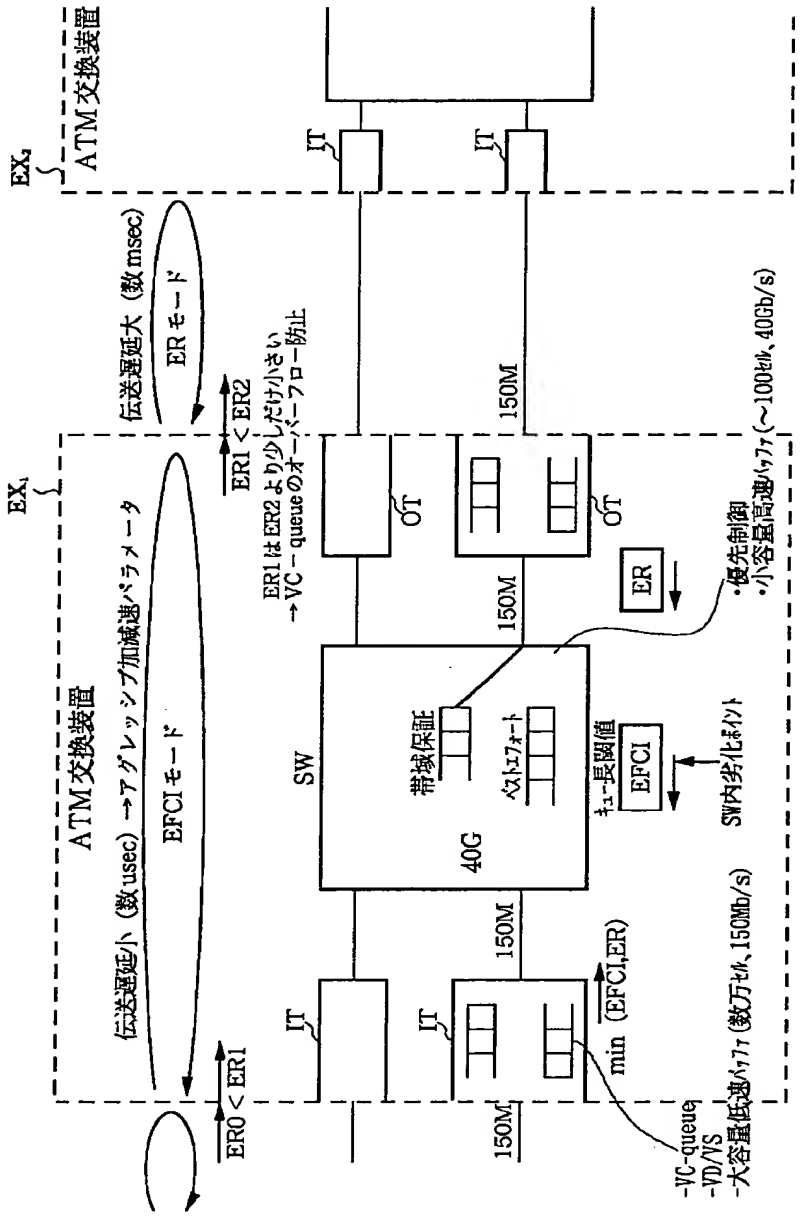
【符号の説明】

１、２、２１、２２　ＲＭセル処理部
３、２３　ＲＭセル生成部
４、２４　ＥＲ演算部
５、２５　読出制御部
３０　ＥＦＣＩ付加部
ＢＵ　出力バッファ
BU_H　高速バッファ
BU_L　低速バッファ
Ｄ　セル分配器
ＥＸ、EX_1、EX_2　ＡＴＭ交換装置
ＩＴ　入力回線対応部
ＯＴ　出力回線対応部
ＳＷ　コアスイッチ

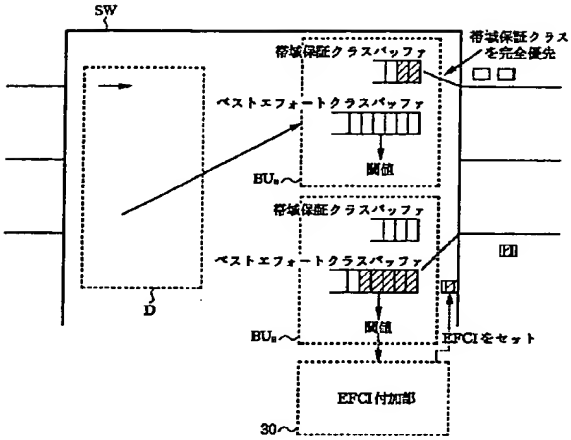
【図３】



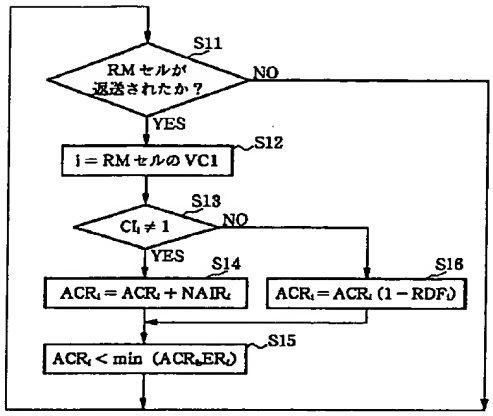
【図１】


EX2
ATM交換装置
EX1
ATM交換装置
伝送遅延大（数msec）
ERモード
伝送遅延小（数usec）→アグレッシブ加減速パラメータ
EFCIモード
ER1 < ER2
ER1はER2より少しだけ小さい
→VC-queueのオーバーフロー防止
ER0 < ER1
IT
OT
150M
SW
40G
帯域保証
ベストエフォート
キュー長閾値
EFCI
ER
優先制御
小容量高速バッファ（～100セル、40Gb/s）
SW内劣化ポイント
min (EFCI,ER)
VC-queue
VD/VS
大容量低速バッファ（数万セル、150Mb/s）

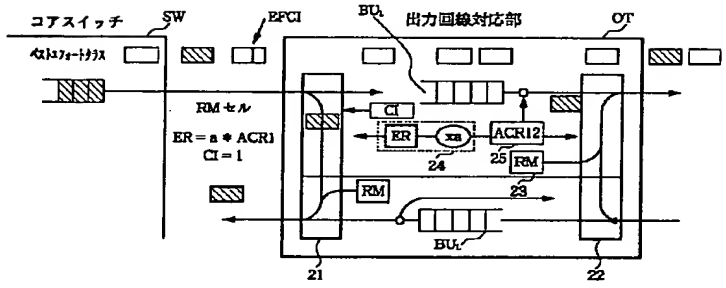
【図２】


SW
帯域保証クラスバッファ
帯域保証クラスを完全優先
ベストエフォートクラスバッファ
閾値
BU₁
帯域保証クラスバッファ
ベストエフォートクラスバッファ
閾値
BU₂
EFCIをセット
EFCI付加部
30
D

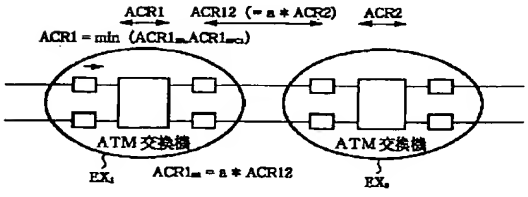
【図６】


S11
RMセルが返送されたか？
NO
YES
i＝RMセルのVCI
S12
S13
CIi≠1
NO
YES
S14
S16
ACRi＝ACRi＋NAIRi
ACRi＝ACRi（1－RDFi）
S15
ACRi＜min（ACR，ERi）

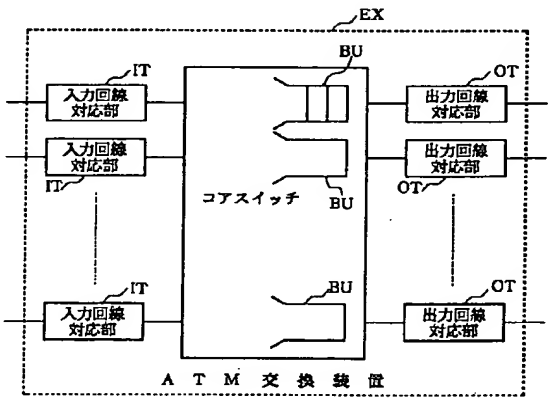
【図４】


コアスイッチ
SW
EFCI
BU₂
出力回線対応部
OT
RMセル
ER＝α＊ACR1
CI＝1
CI
ER
ACR12
24
25
RM
23
RM
BUi
21
22

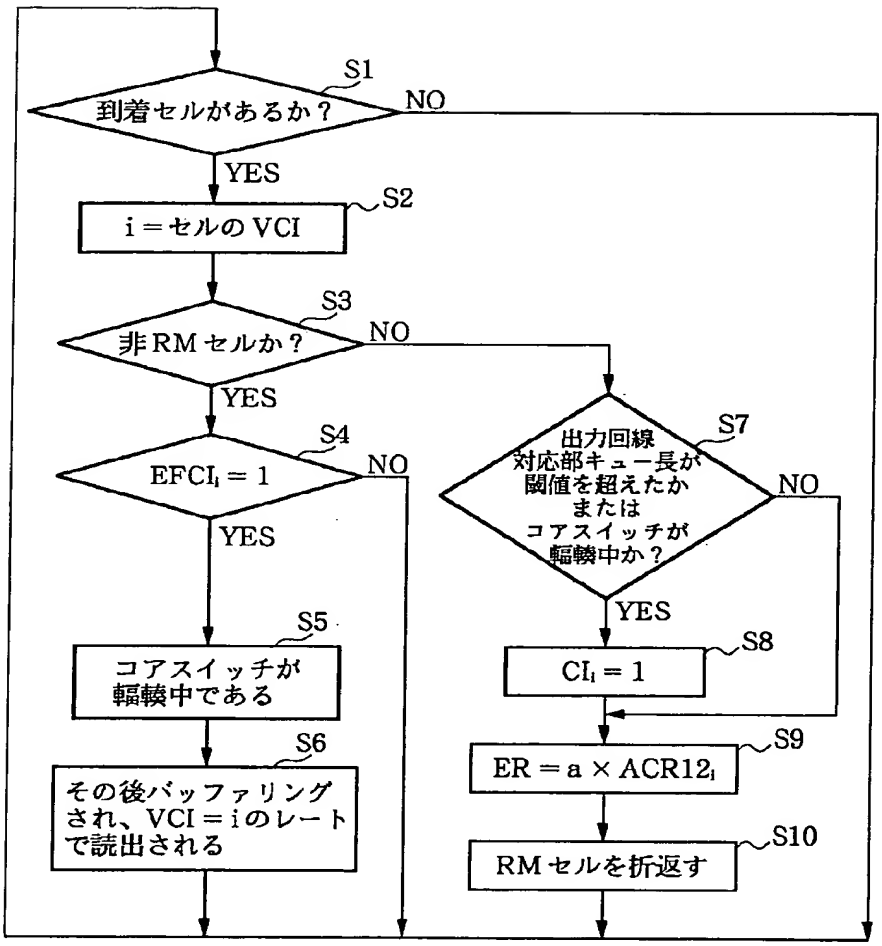
【図７】


ACR1
ACR12（＝α＊ACR2）
ACR2
ACR1＝min（ACR1m，ACR1m-1）
ATM交換機
ATM交換機
EX₁
ACR1m＝α＊ACR12
EX₂

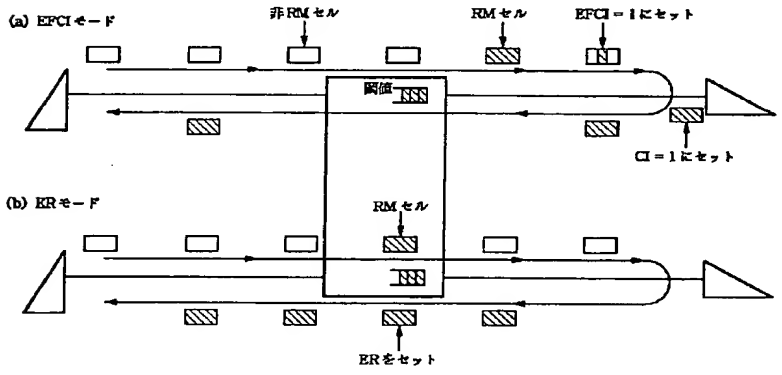
【図８】


EX
BU
IT
入力回線対応部
OT
出力回線対応部
コアスイッチ
ATM交換装置

【図5】


S1
到着セルがあるか？
NO
YES
S2
i＝セルのVCI
S3
非RMセルか？
NO
YES
S4
EFCIi＝1
NO
YES
S5
コアスイッチが
輻輳中である
S6
その後バッファリング
され、VCI＝iのレート
で読出される
S7
出力回線
対応部キュー長が
閾値を超えたか
または
コアスイッチが
輻輳中か？
NO
YES
S8
CIi＝1
S9
ER＝a×ACR12i
S10
RMセルを折返す

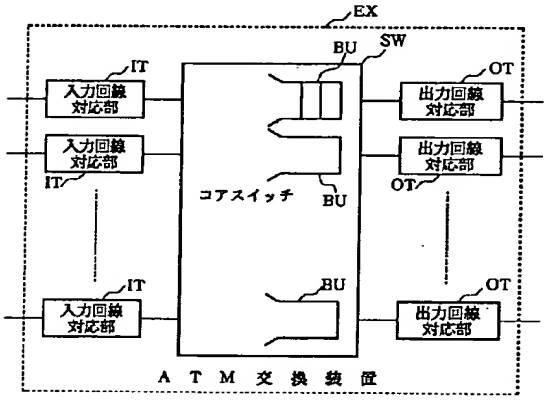
【図9】


(a) EFCIモード
非RMセル
RMセル
EFCI＝1にセット
閾値
CI＝1にセット
(b) ERモード
RMセル
ERをセット

【公報種別】特許法第１７条の２の規定による補正の掲載
【部門区分】第７部門第３区分
【発行日】平成１１年（１９９９）１０月２９日

【公開番号】特開平９－２２４０３３
【公開日】平成９年（１９９７）８月２６日
【年通号数】公開特許公報９－２２４１
【出願番号】特願平８－２９５４５
【国際特許分類第６版】
H04L 12/28
H04Q 3/00
【ＦＩ】
H04L 11/20 G
H04Q 3/00

【手続補正書】
【提出日】平成１１年１月４日
【手続補正１】
【補正対象書類名】図面
【補正対象項目名】図８
【補正方法】変更
【補正内容】
【図８】



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is used for ATM (Asynchronous Transfer Mode: Asynchronous Transfer Mode). This invention relates to the congestion-control technique of an ATM communication network.
[0002]
[Description of the Prior Art] The conventional ATM swap device is explained with reference to drawing 8 . Drawing 8 is the conceptual diagram of the conventional ATM swap device. An ATM swap device consists of two or more input circuit corresponding points IT, output circuit corresponding points OT, and core switches SW. The core switch SW transmits the cel sent out from all the input circuit corresponding points IT for every 1 cel time amount to the desired output circuit corresponding point OT according to the contents of the cel header. When the cel which aims at the same output circuit corresponding point OT from two or more input circuit corresponding points IT is inputted into coincidence here, queuing occurs in the output buffer BU of the core switch SW. Thus, in the conventional ATM swap device, the output buffer BU of the core switch SW becomes the point which congestion generates.
[0003] Drawing 9 is drawing explaining the rate control by ABR (Available Bit Rate) in the conventional ATM network. In the process which sends out and wears RM (Resouce Management) cel from a ** side terminal, turns up RM cel by the side, and returns to a ** side, the end of the side edge from a twist controls the sending-out rate of a cel by ABR to carry the control information according to the congestion condition of a network in RM cel. Thus, in ABR, the control loop for wearing with a ** side terminal and calculating the sending-out rate of a cel in between in the end of a side edge is formed of transmission and reception of RM cel. It is related with the control approach of a cel sending-out rate, and they are EFCI (Explicit Forward Congestion Indication) mode and ER (Explicit Rate). There is the mode.
[0004] In order to show congestion information in RM cel which sets and wears the EFCI field of a cel, notifies in the end of a side edge in order to show having carried out congestion when detecting congestion in EFCI mode by the output buffer of the core switch of an ATM swap device within the net, as shown in drawing 9 (a), and wears, and the end of a side edge turns up to a ** side, CI field is set and it notifies to a ** side terminal. The sending-out rate of the cel of a ** side terminal will be decreased according to predetermined percentage reduction, if it is made to go up according to the predetermined R/C and CI field is set, unless CI field of RM cel which wears and is turned up from the end of a side edge is set.
[0005] In ER mode, as shown in drawing 9 (b), when detecting congestion by the output buffer of the core switch of an ATM swap device within the net, ER information, i.e., sending-out rate assignment information, is specified in RM cel, and the sending-out rate of a cel is shown in a ** side terminal. A value is calculated for every VC from two conditions of the sending-out rate assignment information at this time maintaining fairness and congestion being settled. That is, in EFCI mode, count of the sending-out rate of a cel is left to a terminal side to the core switch of an ATM swap device within the net which carried out congestion calculating the sending-out rate of the cel for every VC in ER mode only by having carried out congestion of the core switch

of an ATM swap device within the net which carried out congestion being shown.
[0006]
[Problem(s) to be Solved by the Invention] If it operates in EFCI mode with a network with the large propagation delay time of a round trip like a public network, since a throughput's not improving and the problem of fairness will become remarkable, having made it more desirable to operate in ER mode understands. However, although ER mode needs to calculate the sending-out rate of a cel for every VC by the output buffer of the core switch of an ATM swap device within the net which carried out congestion, since the core switch of an ATM swap device within the net generally operates at high speed, it is difficult [it] to calculate the cel sending-out rate for every VC. The difficulty will become remarkable if the scale of an ATM swap device becomes large especially. Moreover, although a mass buffer is needed in order to obtain a high throughput as a propagation delay becomes large, generally it is difficult for the core switch which operates at high speed to arrange a mass buffer.
[0007] moreover, an ATM network -- setting -- not only ABR but CBR (Constant Bit Rate), and VBR (Variable Bit Rate) etc. -- a class of service exists and they need to guarantee that it is not influenced by the band by ABR traffic.
[0008] This invention is carried out to such a background, and it aims at offering the ATM swap device which can maintain a high throughput and fairness, without complicating the configuration and actuation of a core switch. This invention aims at offering the ATM swap device which can perform the congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually.
[0009]
[Means for Solving the Problem] In each output circuit of a core switch, the buffer for band guarantee classes is transmitted by full priority. That is, as long as a cel is in the buffer of a band guarantee class, the buffer of a band guarantee class is served, and only when the buffer of a band guarantee class is empty, the buffer of a best effort class is served.
[0010] If the load of a best effort class becomes high, since the queue length of the buffer of a best effort class is extended, if a fixed threshold with queue length is exceeded, the EFCI (Explicit Forward Congestion Indication) field of a passage cel will be set.
[0011] Since it will get to know that the output buffer of a core switch is carrying out congestion if EFCI is set to the cel from the core switch in the output circuit corresponding point, when RM cel is sent out from an input circuit corresponding point, the purport which is in a congestion condition is set and turned up to congestion display field. Moreover, in that case, also when the queue length of the buffer of an output circuit corresponding point is over the threshold, the purport which is in a congestion condition is set and turned up to congestion display field. Moreover, an output circuit corresponding point generates RM cel for every several copies fixed cel fault, sets the cel sending-out rate from a buffer to the ER field, and sends it out to a latter network. According to the value of the congestion display field of RM cel turned up from the latter network, the cel sending-out rate from a buffer is adjusted.
[0012] At an input circuit corresponding point, if RM cel which notifies the purport which is in a congestion condition is returned from an output circuit corresponding point, the cel sending-out rate from a buffer will be decreased by predetermined percentage reduction. Moreover, if RM cel does not show the congestion condition, a cel sending-out rate is raised by the predetermined R/C. Moreover, an input circuit corresponding point sets and turns up the purport which is in a congestion condition to the congestion display field of RM cel sent out from the network of the preceding paragraph, when the queue length of a buffer exceeds a threshold.
[0013] In case RM cel transmitted from the output circuit corresponding point and the input circuit corresponding point is turned up, in addition to setting a value to a congestion display field, what multiplied the cel sending-out rate by the predetermined rate from the buffer of an output circuit corresponding point is set to ER field of RM cel, and is turned up. Moreover, a cel is sent out from a buffer in the one where the rate set as ER field of the cel sending-out rate from a buffer and RM cel calculated according to the value of the congestion display field of RM cel turned up from the latter network is smaller.
[0014] At an input circuit corresponding point, in case a cel sending-out rate is calculated, a cel

sending-out rate is set up with the value below the value of ER field of RM cel returned from the output circuit corresponding point. Moreover, in case an input circuit corresponding point turns up RM cel sent out from the network of the preceding paragraph, in addition to setting a congestion display field, it sets the value which multiplied ER field by the predetermined rate from the buffer at the read-out rate, and turns up RM cel on the network of the preceding paragraph.
[0015] Thus, by controlling, a cel sending-out rate is low stopped as it goes back to an upper node, and it can avoid lapsing into a congestion condition.
[0016] That is, this invention is an ATM swap device and is the ATM swap device with which it had the core switch (SW) which has a high-speed buffer according to output circuit, and a means to distribute an input cel according to the destination of an input cel at this buffer, two or more input circuit corresponding points (IT) which have a low speed buffer in the input side of this core switch were prepared, and two or more output circuit corresponding points (OT) which have a low speed buffer in the output side of this core switch were prepared.
[0017] The place by which it is characterized [of this invention] here to said input circuit corresponding point (IT) The means which carries sending-out rate assignment information (ER information) in RM cel which comes from an input circuit, and is turned up towards the generating origin of the RM cel, It has a means to turn and send out new RM cel to said core switch for a fixed number of cel passage of every. To said output circuit corresponding point (OT) The means which carries congestion information in RM cel which comes from a core switch, and is turned up on said core switch towards the generating origin of the RM cel, It has a means to control the rate of the cel which sends out new RM cel to said output circuit according to the sending-out rate assignment information (ER information) carried in this RM cel turned up by the input circuit corresponding point of a means to send out to an output circuit, and the latter part, for every fixed cel passage. It has a means to add the information (EFCI information) which shows the existence of congestion to the cel to pass according to the queue length of said high-speed buffer to said core switch (SW). Said output circuit corresponding point (OT) is equipped with a means to carry the sending-out rate assignment information (ER information) in RM cel which calculates and turns up the information (EFCI information) which shows the existence of the congestion added to the cel which comes from said core switch. It is in the place equipped with a means to control the rate of the cel sent out to said core switch according to the sending-out rate assignment information (ER information) carried in RM cel turned up from said output circuit corresponding point by said input circuit corresponding point (IT).
[0018] Thereby, a high throughput and fairness can be maintained, without complicating the configuration and actuation of a core switch.
[0019] As for a means for two or more said high-speed buffers to be formed corresponding to the priority of a cel, and to add said information, it is desirable for priority to add the information which shows the second place of the existence of congestion according to the queue length of subsequent high-speed buffers.
[0020] The congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually by this can be performed.
[0021] Said output circuit corresponding point (OT) As for the sending-out rate assignment information (ER information) carried in RM cel which reaches or is turned up by said input circuit corresponding point (IT), it is desirable that it is the late rate which multiplied the acceptable rate judged from the queue length of the low speed buffer of the circuit corresponding point by the rate of a constant ratio.
[0022] Thereby, a cel sending-out rate is low stopped as it goes back to an upper node, and it can avoid lapsing into a congestion condition.
[0023] As for a means to judge the queue length of each low speed buffer of said input circuit corresponding point (IT) and said output circuit corresponding point (OT), and the discernment means of said RM cel, being prepared in virtual channel correspondence is desirable.
[0024] Thereby, a fine congestion control can be performed to virtual channel correspondence.
[0025]
[Embodiment of the Invention]

[0026]
[Example] The configuration of this invention example is explained with reference to drawing 1 thru/or drawing 4 . Drawing 1 is the whole this invention example block diagram. Drawing 2 is the block block diagram of a core switch. Drawing 3 is the block block diagram of an input circuit corresponding point. Drawing 4 is the block block diagram of an output circuit corresponding point.
[0027] the ATM swap device EX1 as shows this invention to drawing 1 , and EX2 it is, as shown in drawing 2 High-speed buffer BUH according to output circuit It is this high-speed buffer BUH according to the destination of an input cel. It has the core switch SW which has the cel distributor D as a means to distribute an input cel. As shown in the input side of this core switch SW at drawing 3 , it is a low speed buffer BUL. Two or more input circuit corresponding points IT which it has are formed. the output side of this core switch SW -- low speed buffer BUL The ATM swap device EX1 with which two or more output circuit corresponding points OT which it has were formed, and EX2 it is .
[0028] The place by which it is characterized [of this invention] here to the input circuit corresponding point IT RM cel processing section 1 and ER operation part 4 as a means which carry ER which is sending-out rate assignment information in RM cel which comes from an input circuit, and are turned up towards the generating origin of the RM cel, It has RM cel generation section 3 as a means and RM cel processing section 2 which turn and send out new RM cel to the core switch SW for a fixed number of cel passage of every. To the output circuit corresponding point OT RM cel processing section 21 as a means which carries congestion information in RM cel which comes from the core switch SW, and is turned up on the core switch SW towards the generating origin of the RM cel, RM cel generation section 23 and RM cel processing section 22 as a means which send out new RM cel to an output circuit for every fixed cel passage, It has the read-out control section 25 as a means to control the rate of the cel sent out to said output circuit according to ER carried in this RM cel turned up by the latter input circuit corresponding point IT. It is the high-speed buffer BUH to the cel passed on the core switch SW. It has the EFCI adjunct 30 as a means to add EFCI which is the information which shows the existence of congestion according to queue length. The output circuit corresponding point OT is equipped with the ER operation part 24 as a means which carries the ER in RM cel calculated and turned up based on EFCI added to the cel which comes from the core switch SW. It is in the place equipped with the read-out control section 5 as a means to control the rate of the cel sent out to the core switch SW according to ER carried in RM cel turned up from the output circuit corresponding point OT by the input circuit corresponding point IT.
[0029] High-speed buffer BUH Corresponding to the priority of a cel, two buffers, a band guarantee class buffer and a best effort class buffer, are formed, and the EFCI adjunct 30 adds EFCI according to the queue length of a best effort class buffer.
[0030] Next, actuation of this invention example is explained. In each output circuit of the core switch SW shown in drawing 2 , a band guarantee class buffer is transmitted by full priority. That is, as long as a cel is in a band guarantee class buffer, a band guarantee class buffer is served, and only when a band guarantee class buffer is empty, a best effort class buffer is served.
[0031] If the load of a best effort class buffer becomes high, since the queue length of a best effort class buffer is extended, if a fixed threshold with queue length is exceeded, the EFCI field of a passage cel will be set.
[0032] The output circuit corresponding point OT shown in drawing 4 receives a cel from the core switch SW. A cel has RM cel and non-RM cel. RM cel is turned up towards the core switch SW -- having -- non-RM cel -- low speed buffer BUL of the output circuit corresponding point OT it buffers -- having -- a latter network -- turning -- the predetermined rate for every VC -- low speed buffer BUL from -- it is sent out -- Although the information carried in RM cel turned up has CI and ER, they are determined by the cel sending-out rate of low speed buffer BUL </SUB> of the congestion condition of the core switch SW, and the output circuit corresponding point OT, respectively.
[0033] Drawing 5 is a flow chart which shows the actuation at the time of cel reception of the

output circuit corresponding point OT. There is a cel which reached the output circuit corresponding point OT (S1), and when the VCI of a cel which arrived is i (S2), the cel is a non-RM cel (S3), and if EFCI is set, it will judge with (S4) and the core switch SW being among congestion (S5). The cel is the low speed buffer BUL of the output circuit corresponding point OT. It is buffered and is read at the predetermined rate for every VC (S6).
[0034] Moreover, the cel which arrived is an RM cel of VCI=i (S3), and it is the low speed buffer BUL of the output circuit corresponding point OT. By queue length having exceeded the threshold, if the core switch SW is among congestion (S7), CIi =1 will be set further (S8), and it is ERi =aACR12i. It sets and (S9) and RM cel are turned up on a core switch (S10). here -- ACR12i Low speed buffer BUL of the output circuit corresponding point OT from -- it is the cel sending-out rate of VCI=i, and a is the safety factor.
[0035] Moreover, in drawing 4 , RM cel generation section 23 of the output circuit corresponding point OT and RM cel processing section 22 send out RM cel to a latter network for every several copies fixed cel fault per VC. that time -- the ER field -- low speed buffer BUL of the cel of the VC concerned from -- a cel sending-out rate is set and it sends out to a latter network. CI field and ER field of RM cel where the read-out control section 25 of the output circuit corresponding point OT was turned up from the latter network -- following -- low speed buffer BUL from -- the sending-out rate of a cel is determined. namely, -- if CI field is set when what was received is RM cel of VCI=i -- low speed buffer BUL from -- sending-out rate ACRi of a cel ACRi =ACRi (1-RDFi) -- (1)
It is if it carries out, and it is made to decrease and CI field is not set. ACRi =ACRi+NAIRi -- (2)
** -- carrying out -- low speed buffer BUL from -- the sending-out rate of a cel is made to increase
[0036] Here, it is RDFi. It is the reduction rate of VCI=i decided in advance, and is NAIRi. It is the increment rate of VCI=i decided in advance. In any case, it is ACRi. ER value ERi carried in turned-up RM cel It is set as a small value.
[0037] RM cel which RM cel processing section 2 of the input circuit corresponding point IT and RM cel generation section 3 which are shown in drawing 3 generated RM cel for every several copies fixed cel fault per VC, sent them out towards the output circuit corresponding point OT, and was turned up by the output circuit corresponding point OT -- receiving -- the read-out control section 5 -- low speed buffer BUL from -- the sending-out rate of a cel is controlled.
[0038] Drawing 6 is the flow chart of the actuation at the time of RM cel reception by which the input circuit corresponding point IT was turned up. since it turns out that the core switch SW is carrying out congestion if CI field is set (S13) when RM cel received when RM cel was returned (S11) is VCI=i (S12) -- low speed buffer BUL from -- sending-out rate ACRi of a cel ACRi =ACRi (1-RDFi) -- (3)
It is made to decrease by carrying out (S16). Here, it is RDFi. It is the reduction rate of VCI=i decided in advance. if CI field is not set (S13), since allowances are still in the core switch SW -- low speed buffer BUL from -- sending-out rate of a cel ACRi =ACRi+NAIRi -- (4)
It is made to increase by carrying out (S14). Here, it is NAIRi. It is the increment rate of VCI=i decided in advance. In any case, it is ACRi. ER value ERi carried in turned-up RM cel It is set as a small value (S15).
[0039] Moreover, in drawing 3 , RM cel processing section 1 of the input circuit corresponding point IT turns to the network of the preceding paragraph RM cel sent out from the network of the preceding paragraph, and turns it up. this time -- ER field -- low speed buffer BUL of the VC concerned from -- the value which multiplied the cel sending-out rate by the predetermined rate is set, and RM cel is turned up on the network of the preceding paragraph.
[0040] The ATM swap device EX1 shown in drawing 1 when the core switch SW, the input circuit corresponding point IT, and the output circuit corresponding point OT operate as mentioned above, and EX2 It functions as follows. The ATM swap device EX1 and EX2 Control of ABR operates in EFCI mode inside. The ATM swap device EX1 and EX2 Since the transit delay is small within equipment, even if it uses EFCI mode, the problem about a throughput fall or fairness is not generated. although it operates in EFCI mode fundamentally -- however, ER field of RM cel -- using -- low speed buffer BUL of the output circuit corresponding point OT from -

- a value smaller than a cel sending-out rate is notified to the input circuit corresponding point IT. thereby -- low speed buffer BUL of the input circuit corresponding point IT from -- a cel sending-out rate -- low speed buffer BUL of the output circuit corresponding point OT from -- it is controlled below at a cel sending-out rate.

[0041] The ATM swap device EX1 and EX2 Control of ABR operates in ER mode in between. latter ATM swap device EX2 since the cel sending-out rate from the low speed buffer BUL of the input circuit corresponding point IT is already known -- ER field of RM cel -- using -- easy -- ATM swap device EX1 of the preceding paragraph it can notify -- ATM swap device EX1 Low speed buffer BUL of the output circuit corresponding point OT from -- a cel sending-out rate can be specified. ATM swap device EX1 Low speed buffer BUL of the output circuit corresponding point OT from -- a cel sending-out rate -- ATM swap device EX2 Low speed buffer BUL of the input circuit corresponding point IT from -- it is set as a value slightly smaller than a cel sending-out rate. thereby -- ATM swap device EX2 Low speed buffer BUL of the input circuit corresponding point IT from -- it becomes possible to control overflow of a cel.

[0042] Drawing 7 is drawing showing the relation of the cel rate of the control loop of ABR within the net. The value of ER is small set up as it goes back to the preceding paragraph from the latter part. Moreover, ATM swap device EX1 It is set as the smaller one of ACR1ER which can be found by ER2 notified from value ACR1EFCI calculated in EFCI mode inside, and the latter part.

[0043] It is effective in being able to simplify the core switch SW, since according to this invention the control loop of ABR is closed in the ATM swap device EX and it is made to operate only in EFCI mode within equipment, and a high throughput and fairness being obtained since the transit delay is small. Since it is made to operate in ER mode between the ATM swap devices EX, a transit delay is able to suppress the fall of the throughput by the large thing low. Since the working speed is not quicker than the core switch SW, commercial memory is usable, and the input circuit corresponding point IT and the output circuit corresponding point OT are the mass low speed buffer BUL. It is possible to be able to realize easily and to suppress the fall of the throughput by a transit delay being large.

[0044] Moreover, since the band guarantee class of CBR or VBR is transmitted by full priority with the core switch SW in the ATM swap device EX, service can be offered, without being influenced of ABR traffic.

[0045]

[Effect of the Invention] As explained above, according to this invention, a high throughput and fairness can be maintained, without complicating the configuration and actuation of a core switch. Moreover, the congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually can be performed.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention is used for ATM (Asynchronous Transfer Mode: Asynchronous Transfer Mode). This invention relates to the congestion-control technique of an ATM communication network.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] The conventional ATM swap device is explained with reference to drawing 8 . Drawing 8 is the conceptual diagram of the conventional ATM swap device. An ATM swap device consists of two or more input circuit corresponding points IT, output circuit corresponding points OT, and core switches SW. The core switch SW transmits the cel sent out from all the input circuit corresponding points IT for every 1 cel time amount to the desired output circuit corresponding point OT according to the contents of the cel header. When the cel which aims at the same output circuit corresponding point OT from two or more input circuit corresponding points IT is inputted into coincidence here, queuing occurs in the output buffer BU of the core switch SW. Thus, in the conventional ATM swap device, the output buffer BU of the core switch SW becomes the point which congestion generates.
[0003] Drawing 9 is drawing explaining the rate control by ABR (Available Bit Rate) in the conventional ATM network. In the process which sends out and wears RM (Resouce Management) cel from a ** side terminal, turns up RM cel by the side, and returns to a ** side, the end of the side edge from a twist controls the sending-out rate of a cel by ABR to carry the control information according to the congestion condition of a network in RM cel. Thus, in ABR, the control loop for wearing with a ** side terminal and calculating the sending-out rate of a cel in between in the end of a side edge is formed of transmission and reception of RM cel. It is related with the control approach of a cel sending-out rate, and they are EFCI (Explicit Forward Congestion Indication) mode and ER (Explicit Rate). There is the mode.
[0004] In order to show congestion information in RM cel which sets and wears the EFCI field of a cel, notifies in the end of a side edge in order to show having carried out congestion when detecting congestion in EFCI mode by the output buffer of the core switch of an ATM swap device within the net, as shown in drawing 9 (a), and wears, and the end of a side edge turns up to a ** side, CI field is set and it notifies to a ** side terminal. The sending-out rate of the cel of a ** side terminal will be decreased according to predetermined percentage reduction, if it is made to go up according to the predetermined R/C and CI field is set, unless CI field of RM cel which wears and is turned up from the end of a side edge is set.
[0005] In ER mode, as shown in drawing 9 (b), when detecting congestion by the output buffer of the core switch of an ATM swap device within the net, ER information, i.e., sending-out rate assignment information, is specified in RM cel, and the sending-out rate of a cel is shown in a ** side terminal.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, a high throughput and fairness can be maintained, without complicating the configuration and actuation of a core switch. Moreover, the congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually can be performed.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] If it operates in EFCI mode with a network with the large propagation delay time of a round trip like a public network, since a throughput's not improving and the problem of fairness will become remarkable, having made it more desirable to operate in ER mode understands. However, although ER mode needs to calculate the sending-out rate of a cel for every VC by the output buffer of the core switch of an ATM swap device within the net which carried out congestion, since the core switch of an ATM swap device within the net generally operates at high speed, it is difficult [it] to calculate the cel sending-out rate for every VC. The difficulty will become remarkable if the scale of an ATM swap device becomes large especially. Moreover, although a mass buffer is needed in order to obtain a high throughput as a propagation delay becomes large, generally it is difficult for the core switch which operates at high speed to arrange a mass buffer.
[0007] moreover, an ATM network -- setting -- not only ABR but CBR (Constant Bit Rate), and VBR (Variable Bit Rate) etc. -- a class of service exists and they need to guarantee that it is not influenced by the band by ABR traffic.
[0008] This invention is carried out to such a background, and it aims at offering the ATM swap device which can maintain a high throughput and fairness, without complicating the configuration and actuation of a core switch. This invention aims at offering the ATM swap device which can perform the congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] In each output circuit of a core switch, the buffer for band guarantee classes is transmitted by full priority. That is, as long as a cel is in the buffer of a band guarantee class, the buffer of a band guarantee class is served, and only when the buffer of a band guarantee class is empty, the buffer of a best effort class is served.
[0010] If the load of a best effort class becomes high, since the queue length of the buffer of a best effort class is extended, if a fixed threshold with queue length is exceeded, the EFCI (Explicit Forward Congestion Indication) field of a passage cel will be set.
[0011] Since it will get to know that the output buffer of a core switch is carrying out congestion if EFCI is set to the cel from the core switch in the output circuit corresponding point, when RM cel is sent out from an input circuit corresponding point, the purport which is in a congestion condition is set and turned up to congestion display field. Moreover, in that case, also when the queue length of the buffer of an output circuit corresponding point is over the threshold, the purport which is in a congestion condition is set and turned up to congestion display field. Moreover, an output circuit corresponding point generates RM cel for every several copies fixed cel fault, sets the cel sending-out rate from a buffer to the ER field, and sends it out to a latter network. According to the value of the congestion display field of RM cel turned up from the latter network, the cel sending-out rate from a buffer is adjusted.
[0012] At an input circuit corresponding point, if RM cel which notifies the purport which is in a congestion condition is returned from an output circuit corresponding point, the cel sending-out rate from a buffer will be decreased by predetermined percentage reduction. Moreover, if RM cel does not show the congestion condition, a cel sending-out rate is raised by the predetermined R/C. Moreover, an input circuit corresponding point sets and turns up the purport which is in a congestion condition to the congestion display field of RM cel sent out from the network of the preceding paragraph, when the queue length of a buffer exceeds a threshold.
[0013] In case RM cel transmitted from the output circuit corresponding point and the input circuit corresponding point is turned up, in addition to setting a value to a congestion display field, what multiplied the cel sending-out rate by the predetermined rate from the buffer of an output circuit corresponding point is set to ER field of RM cel, and is turned up. Moreover, a cel is sent out from a buffer in the one where the rate set as ER field of the cel sending-out rate from a buffer and RM cel calculated according to the value of the congestion display field of RM cel turned up from the latter network is smaller.
[0014] At an input circuit corresponding point, in case a cel sending-out rate is calculated, a cel sending-out rate is set up with the value below the value of ER field of RM cel returned from the output circuit corresponding point. Moreover, in case an input circuit corresponding point turns up RM cel sent out from the network of the preceding paragraph, in addition to setting a congestion display field, it sets the value which multiplied ER field by the predetermined rate from the buffer at the read-out rate, and turns up RM cel on the network of the preceding paragraph.
[0015] Thus, by controlling, a cel sending-out rate is low stopped as it goes back to an upper node, and it can avoid lapsing into a congestion condition.
[0016] That is, this invention is an ATM swap device and is the ATM swap device with which it

had the core switch (SW) which has a high-speed buffer according to output circuit, and a means to distribute an input cel according to the destination of an input cel at this buffer, two or more input circuit corresponding points (IT) which have a low speed buffer in the input side of this core switch were prepared, and two or more output circuit corresponding points (OT) which have a low speed buffer in the output side of this core switch were prepared.
[0017] The place by which it is characterized [of this invention] here to said input circuit corresponding point (IT) The means which carries sending-out rate assignment information (ER information) in RM cel which comes from an input circuit, and is turned up towards the generating origin of the RM cel, It has a means to turn and send out new RM cel to said core switch for a fixed number of cel passage of every. To said output circuit corresponding point (OT) The means which carries congestion information in RM cel which comes from a core switch, and is turned up on said core switch towards the generating origin of the RM cel, It has a means to control the rate of the cel which sends out new RM cel to said output circuit according to the sending-out rate assignment information (ER information) carried in this RM cel turned up by the input circuit corresponding point of a means to send out to an output circuit, and the latter part, for every fixed cel passage. It has a means to add the information (EFCI information) which shows the existence of congestion to the cel to pass according to the queue length of said high-speed buffer to said core switch (SW). Said output circuit corresponding point (OT) is equipped with a means to carry the sending-out rate assignment information (ER information) in RM cel which calculates and turns up the information (EFCI information) which shows the existence of the congestion added to the cel which comes from said core switch. It is in the place equipped with a means to control the rate of the cel sent out to said core switch according to the sending-out rate assignment information (ER information) carried in RM cel turned up from said output circuit corresponding point by said input circuit corresponding point (IT).
[0018] Thereby, a high throughput and fairness can be maintained, without complicating the configuration and actuation of a core switch.
[0019] As for a means for two or more said high-speed buffers to be formed corresponding to the priority of a cel, and to add said information, it is desirable for priority to add the information which shows the second place of the existence of congestion according to the queue length of subsequent high-speed buffers.
[0020] The congestion control to which the class of service prepared according to the priority of a cel does not interfere mutually by this can be performed.
[0021] Said output circuit corresponding point (OT) As for the sending-out rate assignment information (ER information) carried in RM cel which reaches or is turned up by said input circuit corresponding point (IT), it is desirable that it is the late rate which multiplied the acceptable rate judged from the queue length of the low speed buffer of the circuit corresponding point by the rate of a constant ratio.
[0022] Thereby, a cel sending-out rate is low stopped as it goes back to an upper node, and it can avoid lapsing into a congestion condition.
[0023] As for a means to judge the queue length of each low speed buffer of said input circuit corresponding point (IT) and said output circuit corresponding point (OT), and the discernment means of said RM cel, being prepared in virtual channel correspondence is desirable.
[0024] Thereby, a fine congestion control can be performed to virtual channel correspondence.
[0025]
[Embodiment of the Invention]

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] The configuration of this invention example is explained with reference to drawing 1 thru/or drawing 4 . Drawing 1 is the whole this invention example block diagram. Drawing 2 is the block block diagram of a core switch. Drawing 3 is the block block diagram of an input circuit corresponding point. Drawing 4 is the block block diagram of an output circuit corresponding point.
[0027] the ATM swap device EX1 as shows this invention to drawing 1 , and EX2 it is, as shown in drawing 2 High-speed buffer BUH according to output circuit It is this high-speed buffer BUH according to the destination of an input cel. It has the core switch SW which has the cel distributor D as a means to distribute an input cel. As shown in the input side of this core switch SW at drawing 3 , it is a low speed buffer BUL. Two or more input circuit corresponding points IT which it has are formed. the output side of this core switch SW -- low speed buffer BUL The ATM swap device EX1 with which two or more output circuit corresponding points OT which it has were formed, and EX2 it is .
[0028] The place by which it is characterized [of this invention] here to the input circuit corresponding point IT RM cel processing section 1 and ER operation part 4 as a means which carry ER which is sending-out rate assignment information in RM cel which comes from an input circuit, and are turned up towards the generating origin of the RM cel, It has RM cel generation section 3 as a means and RM cel processing section 2 which turn and send out new RM cel to the core switch SW for a fixed number of cel passage of every. To the output circuit corresponding point OT RM cel processing section 21 as a means which carries congestion information in RM cel which comes from the core switch SW, and is turned up on the core switch SW towards the generating origin of the RM cel, RM cel generation section 23 and RM cel processing section 22 as a means which send out new RM cel to an output circuit for every fixed cel passage, It has the read-out control section 25 as a means to control the rate of the cel sent out to said output circuit according to ER carried in this RM cel turned up by the latter input circuit corresponding point IT. It is the high-speed buffer BUH to the cel passed on the core switch SW. It has the EFCI adjunct 30 as a means to add EFCI which is the information which shows the existence of congestion according to queue length. The output circuit corresponding point OT is equipped with the ER operation part 24 as a means which carries the ER in RM cel calculated and turned up based on EFCI added to the cel which comes from the core switch SW. It is in the place equipped with the read-out control section 5 as a means to control the rate of the cel sent out to the core switch SW according to ER carried in RM cel turned up from the output circuit corresponding point OT by the input circuit corresponding point IT.
[0029] High-speed buffer BUH Corresponding to the priority of a cel, two buffers, a band guarantee class buffer and a best effort class buffer, are formed, and the EFCI adjunct 30 adds EFCI according to the queue length of a best effort class buffer.
[0030] Next, actuation of this invention example is explained. In each output circuit of the core switch SW shown in drawing 2 , a band guarantee class buffer is transmitted by full priority. That is, as long as a cel is in a band guarantee class buffer, a band guarantee class buffer is served, and only when a band guarantee class buffer is empty, a best effort class buffer is served.

[0031] If the load of a best effort class buffer becomes high, since the queue length of a best effort class buffer is extended, if a fixed threshold with queue length is exceeded, the EFCI field of a passage cel will be set.
[0032] The output circuit corresponding point OT shown in drawing 4 receives a cel from the core switch SW. A cel has RM cel and non-RM cel. RM cel is turned up towards the core switch SW -- having -- non-RM cel -- low speed buffer BUL of the output circuit corresponding point OT it buffers -- having -- a latter network -- turning -- the predetermined rate for every VC -- low speed buffer BUL from -- although the information carried in RM cel which is sent out, and which is turned up has CI and ER -- respectively -- them -- the congestion condition of the core switch SW, and low speed buffer BUL of the output circuit corresponding point OT It is determined by the cel sending-out rate.
[0033] Drawing 5 is a flow chart which shows the actuation at the time of cel reception of the output circuit corresponding point OT. There is a cel which reached the output circuit corresponding point OT (S1), and when the VCI of a cel which arrived is i (S2), the cel is a non-RM cel (S3), and if EFCI is set, it will judge with (S4) and the core switch SW being among congestion (S5). The cel is the low speed buffer BUL of the output circuit corresponding point OT. It is buffered and is read at the predetermined rate for every VC (S6).
[0034] Moreover, the cel which arrived is an RM cel of VCI=i (S3), and it is the low speed buffer BUL of the output circuit corresponding point OT. By queue length having exceeded the threshold, if the core switch SW is among congestion (S7), CIi =1 will be set further (S8), and it is ERi =aACR12i. It sets and (S9) and RM cel are turned up on a core switch (S10). here -- ACR12i Low speed buffer BUL of the output circuit corresponding point OT from -- it is the cel sending-out rate of VCI=i, and a is the safety factor.
[0035] Moreover, in drawing 4 , RM cel generation section 23 of the output circuit corresponding point OT and RM cel processing section 22 send out RM cel to a latter network for every several copies fixed cel fault per VC. that time -- the ER field -- low speed buffer BUL of the cel of the VC concerned from -- a cel sending-out rate is set and it sends out to a latter network. CI field and ER field of RM cel where the read-out control section 25 of the output circuit corresponding point OT was turned up from the latter network -- following -- low speed buffer BUL from -- the sending-out rate of a cel is determined. namely, -- if CI field is set when what was received is RM cel of VCI=i -- low speed buffer BUL from -- sending-out rate ACRi of a cel ACRi =ACRi (1-RDFi) -- (1)
It is if it carries out, and it is made to decrease and CI field is not set. ACRi =ACRi+NAIRi -- (2)
** -- carrying out -- low speed buffer BUL from -- the sending-out rate of a cel is made to increase
[0036] Here, it is RDFi. It is the reduction rate of VCI=i decided in advance, and is NAIRi. It is the increment rate of VCI=i decided in advance. In any case, it is ACRi. ER value ERi carried in turned-up RM cel It is set as a small value.
[0037] RM cel which RM cel processing section 2 of the input circuit corresponding point IT and RM cel generation section 3 which are shown in drawing 3 generated RM cel for every several copies fixed cel fault per VC, sent them out towards the output circuit corresponding point OT, and was turned up by the output circuit corresponding point OT -- receiving -- the read-out control section 5 -- low speed buffer BUL from -- the sending-out rate of a cel is controlled.
[0038] Drawing 6 is the flow chart of the actuation at the time of RM cel reception by which the input circuit corresponding point IT was turned up. since it turns out that the core switch SW is carrying out congestion if CI field is set (S13) when RM cel received when RM cel was returned (S11) is VCI=i (S12) -- low speed buffer BUL from -- sending-out rate ACRi of a cel ACRi =ACRi (1-RDFi) -- (3)
It is made to decrease by carrying out (S16). Here, it is RDFi. It is the reduction rate of VCI=i decided in advance. if CI field is not set (S13), since allowances are still in the core switch SW -- low speed buffer BUL from -- sending-out rate of a cel ACRi =ACRi+NAIRi -- (4)
It is made to increase by carrying out (S14). Here, it is NAIRi. It is the increment rate of VCI=i decided in advance. In any case, it is ACRi. ER value ERi carried in turned-up RM cel It is set as a small value (S15).

[0039] Moreover, in drawing 3 , RM cel processing section 1 of the input circuit corresponding point IT turns to the network of the preceding paragraph RM cel sent out from the network of the preceding paragraph, and turns it up. this time -- ER field -- low speed buffer BUL of the VC concerned from -- the value which multiplied the cel sending-out rate by the predetermined rate is set, and RM cel is turned up on the network of the preceding paragraph.
[0040] The ATM swap device EX1 shown in drawing 1 when the core switch SW, the input circuit corresponding point IT, and the output circuit corresponding point OT operate as mentioned above, and EX2 It functions as follows. The ATM swap device EX1 and EX2 Control of ABR operates in EFCI mode inside. The ATM swap device EX1 and EX2 Since the transit delay is small within equipment, even if it uses EFCI mode, the problem about a throughput fall or fairness is not generated. although it operates in EFCI mode fundamentally -- however, ER field of RM cel -- using -- low speed buffer BUL of the output circuit corresponding point OT from -- a value smaller than a cel sending-out rate is notified to the input circuit corresponding point IT. thereby -- low speed buffer BUL of the input circuit corresponding point IT from -- a cel sending-out rate -- low speed buffer BUL of the output circuit corresponding point OT from -- it is controlled below at a cel sending-out rate.
[0041] The ATM swap device EX1 and EX2 Control of ABR operates in ER mode in between. latter ATM swap device EX2 since the cel sending-out rate from the low speed buffer BUL of the input circuit corresponding point IT is already known -- ER field of RM cel -- using -- easy -- ATM swap device EX1 of the preceding paragraph it can notify -- ATM swap device EX1 Low speed buffer BUL of the output circuit corresponding point OT from -- a cel sending-out rate can be specified. ATM swap device EX1 Low speed buffer BUL of the output circuit corresponding point OT from -- a cel sending-out rate -- ATM swap device EX2 Low speed buffer BUL of the input circuit corresponding point IT from -- it is set as a value slightly smaller than a cel sending-out rate. thereby -- ATM swap device EX2 Low speed buffer BUL of the input circuit corresponding point IT from -- it becomes possible to control overflow of a cel.
[0042] Drawing 7 is drawing showing the relation of the cel rate of the control loop of ABR within the net. The value of ER is small set up as it goes back to the preceding paragraph from the latter part. Moreover, ATM swap device EX1 It is set as the smaller one of ACR1ER which can be found by ER2 notified from value ACR1EFCI calculated in EFCI mode inside, and the latter part.
[0043] It is effective in being able to simplify the core switch SW, since according to this invention the control loop of ABR is closed in the ATM swap device EX and it is made to operate only in EFCI mode within equipment, and a high throughput and fairness being obtained since the transit delay is small. Since it is made to operate in ER mode between the ATM swap devices EX, a transit delay is able to suppress the fall of the throughput by the large thing low. Since the working speed is not quicker than the core switch SW, commercial memory is usable, and the input circuit corresponding point IT and the output circuit corresponding point OT are the mass low speed buffer BUL. It is possible to be able to realize easily and to suppress the fall of the throughput by a transit delay being large.
[0044] Moreover, since the band guarantee class of CBR or VBR is transmitted by full priority with the core switch SW in the ATM swap device EX, service can be offered, without being influenced of ABR traffic.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The whole this invention example block diagram.
[Drawing 2] The block block diagram of a core switch.
[Drawing 3] The block block diagram of an input circuit corresponding point.
[Drawing 4] The block block diagram of an output circuit corresponding point.
[Drawing 5] The flow chart which shows the actuation at the time of cel reception of an output circuit corresponding point.
[Drawing 6] The flow chart of the actuation at the time of RM cel reception by which the input circuit corresponding point was turned up.
[Drawing 7] Drawing showing the relation of the cel rate of the control loop of ABR within the net.
[Drawing 8] The conceptual diagram of the conventional ATM swap device.
[Drawing 9] Drawing explaining the rate control by ABR in the conventional ATM network.
[Description of Notations]
1, 2, 21, 22 RM cel processing section
3 23 RM cel generation section
4 24 ER operation part
5 25 Read-out control section
30 EFCI Adjunct
BU Output buffer
BUH High-speed buffer
BUL Low speed buffer
D Cel distributor
EX, EX1, EX2 ATM swap device
IT Input circuit corresponding point
OT Output circuit corresponding point
SW Core switch

[Translation done.]

* NOTICES *

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 3rd partition of the 7th section
[Publication date] October 29, Heisei 11 (1999)

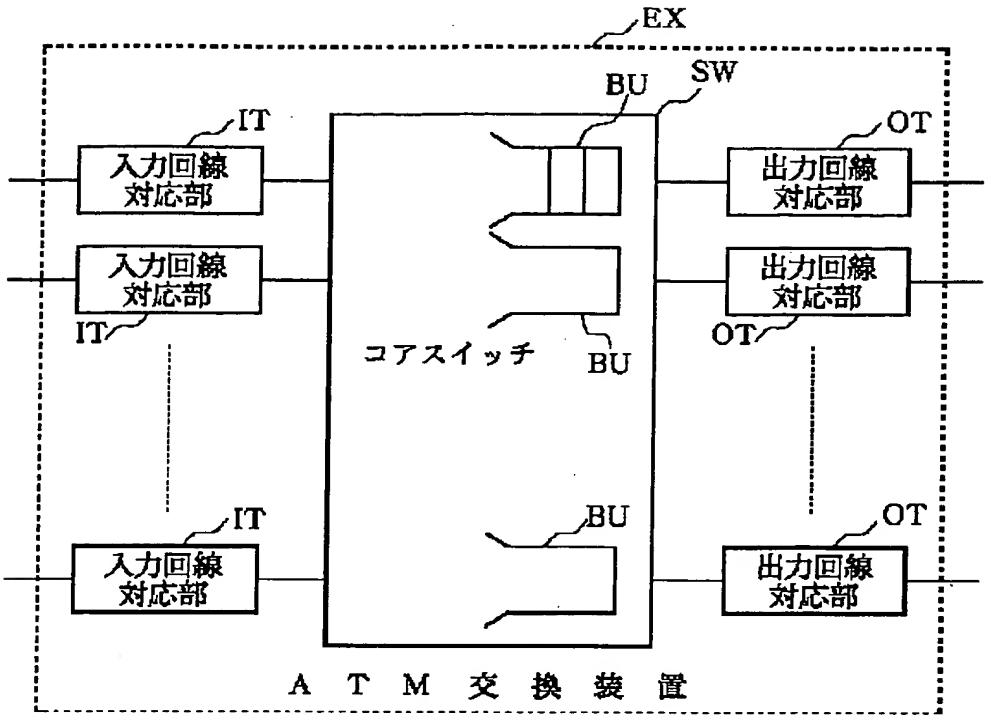
[Publication No.] Publication number 9-224033
[Date of Publication] August 26, Heisei 9 (1997)
[Annual volume number] Open patent official report 9-2241
[Application number] Japanese Patent Application No. 8-29545
[International Patent Classification (6th Edition)]

H04L 12/28
H04Q 3/00

[FI]

H04L 11/20 G
H04Q 3/00

[Procedure revision]
[Filing Date] January 4, Heisei 11
[Procedure amendment 1]
[Document to be Amended] DRAWINGS
[Item(s) to be Amended] drawing 8
[Method of Amendment] Modification
[Proposed Amendment]
[Drawing 8]



[Translation done.]